## **AMENDMENTS TO THE CLAIMS**

1. (Currently Amended) A coordinate input apparatus, comprising:

a display panel provided with a plurality of X interconnecting lines and a plurality of Y interconnecting lines disposed to intersect with each other in a matrix fashion;

display drive circuits for supplying drive signals to the X and Y interconnecting lines in a display drive mode;

closed loop forming circuits disposed at two opposite ends of the display panel and at another two opposite ends of the display panel;

switching circuits connected to a terminal of each of the X and Y interconnecting lines, said switching circuits connecting the X or Y interconnecting lines to the display drive circuits in the display drive mode and to the closed loop forming circuits in a coordinate detection drive mode; and

a switching circuit for connecting the X and Y interconnecting lines to a display drive circuit in a display drive mode and for connecting the X and Y interconnecting lines to a closed-loop forming circuit in a coordinate detection drive mode;

the closed loop forming circuit switchably connecting a predetermined number of the X interconnecting lines or a predetermined number of the Y interconnecting lines to form a closed loop in the coordinate detection drive mode; and

a detection circuit for detecting [[a]] signals outputted from the closed loop forming circuits in the coordinate detection drive mode in response to a position indicator for indicating a position in a coordinate input area of the display panel where the X interconnecting lines and the Y interconnecting lines are disposed in the matrix fashion;

wherein the closed loop is a multiple closed loop, in the coordinate detection drive mode,

the closed-loop forming circuits disposed at two ends of the display panel connect at least a pair of terminals of the X interconnecting lines in each end to form a multiple closed loop of the X interconnecting lines, and

the closed loop forming circuits disposed at another two ends of the display panel connect at least a pair of terminals of the Y interconnecting lines at each end to form a multiple closed loop of the Y interconnecting lines.

2. (Original) An apparatus according to Claim 1, wherein the closed loop includes a switch circuit for selecting first to four X interconnecting lines from the plurality of X interconnecting lines so that:

a first terminal of the first X interconnecting line is connected with a first terminal of the second X interconnecting line,

a first terminal of the third X interconnecting line is connected with a first output terminal,

a second terminal of the third X interconnecting line is connected with a second terminal of the first X interconnecting line,

a first terminal of the fourth X interconnecting line is connected with a second output terminal, and

a second terminal of the fourth X interconnecting line is connected with a second terminal of the second X interconnecting line.

3. (Original) An apparatus according to Claim 2, wherein the closed loop includes a switch circuit for selecting first to four Y interconnecting lines from the plurality of Y interconnecting lines so that:

a first terminal of the first Y interconnecting line is connected with a first terminal of the second Y interconnecting line,

a first terminal of the third Y interconnecting line is connected with a first output terminal,

a second terminal of the third Y interconnecting line is connected with a second terminal of the first Y interconnecting line,

a first terminal of the fourth Y interconnecting line is connected with a second output terminal, and

a second terminal of the fourth Y interconnecting line is connected with a second terminal of the second Y interconnecting line.

- 4. (Original) An apparatus according to Claim 1, wherein the closed loop is sequentially formed at a constant pitch on the matrix of the X and Y interconnecting lines with a lapse of time.
- 5. (Original) An apparatus according to Claim 1, wherein on the matrix of the X and Y interconnecting lines, a closed loop formed timewise previously and a subsequent closed loop formed after the closed loop are selected to have an embedded structure.

## 6 and 7. (Canceled)

8. (Previously Presented) An apparatus according to Claim 1, wherein the display panel has a memory characteristic.

Application No. 10/557,520 Response dated February 17, 2009 In reply to Final Office Action of November 17, 2008

9. (Original) An apparatus according to Claim 8, wherein the display panel is an electrophoretic display panel.